ABSTRACT OF THE DISCLOSURE

An apparatus comprising a circuit configured to be tested and a plurality of test blocks within the circuit. Each of the test blocks generally comprises (i) a plurality of sequential elements and (ii) a plurality of logic elements. Each of the test blocks are configured to operate (a) in a first mode comprising a shift mode and (b) a second mode comprising a capture mode. The shift mode generally operates with multiple scan clocks that are clocked simultaneously. The capture mode generally operates with multiple scan clocks, but only one of which is toggled at a time.